AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A constant voltage generating circuit comprising:

a ~~group~~ plurality of first bipolar transistors ~~including~~ , a number of said plurality of first bipolar transistors being n (an integer; 2≤n), each of the plurality of first bipolar transistors having an emitter area;

a ~~group~~ plurality of second bipolar transistors including n second bipolar transistors each having [[a]] an associated ~~larger~~ emitter area greater than the emitter area of each of the plurality of first bipolar transistors;

differential voltage generating means for generating a differential voltage between a voltage equal to a sum of base emitter voltages of said n first bipolar transistors and a sum of base emitter voltages of said n second bipolar transistors; and

voltage amplification adding means for amplifying said differential voltage and adding the amplified voltage to the base emitter voltage of one of said [[group]] plurality of second bipolar transistors to output a constant voltage independent of temperature and substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors.

2. (Original) The constant voltage generating circuit as claimed in claim 1, wherein said differential voltage generating means includes a differential amplifier, and an offset voltage at said differential amplifier in input equivalent has a primary temperature characteristic.

3. (Currently Amended) A constant voltage generating circuit comprising:

a ~~group~~ plurality of first bipolar transistors ~~including~~ , a number of said plurality of first bipolar transistors being n (an integer; $2 \leq n$) , each of the plurality of first bipolar transistors having an emitter area;

a ~~group~~ plurality of second bipolar transistors including n second bipolar transistors each having [[a]] an associated ~~larger~~ emitter area greater than the emitter area of each of the plurality of the first bipolar transistors;

differential voltage generating means for generating a differential voltage between a voltage equal to a sum of base emitter voltages of said n first bipolar transistors and a sum of base emitter voltages of said n second bipolar transistors; and

voltage amplification adding means including a differential amplifier in which an offset voltage in input equivalent has a primary temperature characteristic, for amplifying said differential voltage and adding the amplified voltage to the sum of the base emitter voltages of ~~said group~~ said n second bipolar transistors to output a constant voltage independent of temperature and substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors.

4. (Currently Amended) A constant voltage generating circuit comprising:

a ~~group~~ plurality of first pnp transistors including n (an integer; $2 \leq n$) first pnp transistors, a collector of each of the plurality of first pnp transistors being grounded, a base of a ~~first of the group~~ one of the plurality of first pnp transistors being grounded, a base of a k (an integer; $2 \leq k \leq n$)-th one of the ~~group~~ plurality of first pnp transistors being connected to an emitter of a (k-1)-th one of the ~~group~~ plurality of first pnp transistors;

a ~~group~~ plurality of second pnp transistors including n second pnp transistors each having ~~a larger~~ an emitter area greater than the first pnp transistors, [[an]] a collector of each of the ~~group~~ plurality of second pnp transistors being grounded, a base of a ~~first of the group~~ first one of the plurality of second pnp transistors being grounded, a collector of each of the ~~group~~ plurality of second pnp transistors being grounded, a base of a k-th one of the ~~group~~ plurality of second pnp transistors except ~~a second~~ for an another one of the ~~group~~ plurality of second pnp transistors being connected to an emitter of a (k-1)-th one of the ~~group~~ plurality of second pnp transistors;

current sources connected to the respective emitters of said ~~group~~ plurality of first pnp transistors and the respective emitters of said ~~group~~ plurality of second pnp transistors, except ~~the first of the group of~~ for a emitter of the first one of the plurality of second pnp transistors to supply currents to the respective pnp transistors of said ~~groups of~~ pluralities of first and second pnp transistors, two resistors being connected in series between the emitter of said ~~first of the group~~ first one of the of plurality of second pnp transistors and the corresponding [[power]] current source, a connection point between the two resistors being connected to the base of said ~~second~~ another one of the ~~group~~ plurality of second pnp transistors; and

current control means including a first input terminal to which the emitter of [[an]] a n-th one of the plurality of first pnp transistors is connected and a second input terminal to which the emitter of [[an]] a n-th one of the plurality of second pnp transistors is connected, the current control means controlling currents from the current sources by outputting a control signal that controls the currents from said current sources so that a potential at said first input terminal and a potential at said second input terminal are the same.

5. (Currently Amended) A constant voltage generating circuit comprising:

a ~~group~~ plurality of first npn transistors including n (an integer; $2 \leq n$) first npn transistors, a base and a collector of each of the plurality of first npn transistors being connected together, an emitter of a [[first]] one of the plurality of first npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of first npn transistors being connected to a collector of a (k-1)-th one of the plurality of first npn transistors;

a ~~group~~ plurality of second npn transistors including n second npn transistors each having ~~a larger~~ an emitter area greater than [[the]] each of the plurality of first npn transistors, a base and a collector of each of said plurality of second npn transistors being connected together, an emitter of a [[first]] one of the plurality of second npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of second npn transistors, except ~~a second~~ an another one of the plurality of second npn transistors being connected to a collector of a (k-1)-th one of the plurality of second npn transistors;

current sources connected to the collector of [[an]] a n-th one of said ~~group~~ plurality of first npn transistors and the collector of [[an]] a n-th one the ~~group~~ plurality of second npn transistors to supply currents to the respective npn transistors of the ~~groups~~ pluralities of first and second npn transistors, said ~~first~~ one of the plurality of second npn transistors being connected to the corresponding current source via two resistors connected in series, a connection point between the two resistors being connected to [[the]] an emitter of said ~~second of the group~~ another one of the plurality of second npn transistors; and

current control means including a first input terminal to which the collector of said n-th one of the plurality of first npn transistors is connected and a second input terminal to which the collector of said n-th one of the plurality of second npn transistors is connected, the current control means controlling currents from said current sources by outputting a control signal that controls the currents from said current sources so that a potential at the first input terminal and a potential at the second input terminal are the same.

6. (Currently Amended) The constant voltage generating circuit as claimed in claim 4 or 5, ~~wherein said~~ further comprising a differential voltage generating means which includes a differential amplifier, and an offset voltage at said differential amplifier in input equivalent has a primary temperature characteristic.

7. (Currently Amended) A constant voltage generating circuit comprising:

a [[group]] plurality of first pnp transistors including n (an integer; 2≤n) first pnp transistors, a collector of each of the plurality of first pnp transistors being grounded, a base of a [[first]] one of the plurality of first pnp transistors being grounded, a base of a k (an integer; 2≤k≤n)-th one of the plurality of first pnp transistors being connected to an emitter of a (k-1)-th one of the plurality of first pnp transistors;

a [[group]] plurality of second pnp transistors including n second pnp transistors each having ~~a larger~~ an emitter area greater than each of the plurality of [[the]] first pnp transistors, [[an]] a collector of each of the plurality of second pnp transistors being grounded, a base of a [[first]] one of the plurality of second pnp transistors being grounded, a base of a k-th one of the plurality of second pnp transistors being connected to an emitter of a (k-1)-th one of the plurality of second pnp transistors;

current sources connected to the respective emitters of said [[group]] plurality of first pnp transistors and the respective emitters of said [[group]] plurality of second pnp transistors except an emitter of the n-th one of the [[group]] plurality of second pnp transistors to supply currents to the respective pnp transistors of said ~~groups~~ pluralities of first and second pnp transistors, two resistors being connected in series between the emitter of said n-th one of the plurality second pnp transistors and the corresponding ~~power~~ current source; and

current control means including a first input terminal to which the emitter of [[an]] a n-th one of the plurality of first pnp transistors is connected, a second input terminal to which a first connection point between said two resistors connected in series is connected, and a differential amplifier, the current control means controlling currents

from said current sources by outputting a control signal that controls the currents from said current sources so that a potential at said first input terminal and a potential at said second input terminal are the same, an offset voltage at the differential amplifier in input equivalent having a primary temperature characteristic and,

wherein a second connection point to one of said two resistors has a constant voltage that is substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors.

8. (Currently Amended) A constant voltage generating circuit comprising:

a [[group]] plurality of first npn transistors including n (an integer; 2≤n) first npn transistors, a base and a collector of each of the plurality of first npn transistors being connected together, an emitter of a [[first]] one of the plurality of first npn transistors being grounded, an emitter of a k (an integer; 2≤k≤n)-th one of the plurality of first npn transistors being connected to a collector of a (k-1)-th one of the plurality of first npn transistors;

a [[group]] plurality of second npn transistors including n second npn transistors each having ~~a larger~~ an emitter area greater than each of the plurality of the first npn transistor, a base and a collector of each of the plurality of second npn transistors being connected together, an emitter of a [[first]] one of the plurality of second npn transistors being grounded, an emitter of a k (an integer; 2≤k≤n)-th one of the plurality of second npn transistors being connected to a collector of a (k-1)-th of the plurality of second npn transistors;

a current source connected to the collector of [[an]] a n-th one of the [[group]] plurality of first npn transistors to supply a current to each of the ~~groups~~ pluralities of first and second npn transistors, two resistors being connected in series between the current source and [[an]] a n-th one of the plurality of second npn transistors; and

current control means comprising a first input terminal including a differential amplifier in which an offset voltage in input equivalent has a primary temperature characteristic, the n-th one of the plurality of first npn transistors being connected to the first input terminal, and a second input terminal to which a first connection point between said two resistors connected in series is connected, the current control means controlling a current from said current source by outputting a control signal that controls the current from said current source so that a potential at said first input terminal and a potential at said second input terminal are the same and,

wherein a second connection point to one of said two resistors has a constant voltage that is substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors.

9. (Currently Amended) The constant voltage generating circuit as claimed in any of claims 4 or 5, ~~wherein said~~ further comprising a differential voltage generating means ~~includes~~ including a differential amplifier, and an offset voltage at said differential amplifier in input equivalent has a primary temperature characteristic,

wherein said differential amplifier has a differential pair including a first npn transistor and a second npn transistor having a larger emitter area than the first npn

transistor, and a first and second current sources ~~that supplies~~ to supply a first and second current to said differential pair,

wherein said differential pair includes a first and second input terminals, said first input terminal is a base of said first npn transistor, and said second input terminal is a base of said second npn transistor, and

wherein an emitter of said first npn transistor is connected to said first current source, and an emitter of said second npn transistor is connected to said second current source, the emitter of said first npn transistor being connected to the emitter of said second npn transistor.

10. (Currently Amended) The constant voltage generating circuit as claimed in any of claims 7 or 8, ~~wherein said~~ further comprising a differential amplifier [[has]] having a differential pair including a first npn transistor and a second npn transistor having a larger emitter area than the first npn transistor, and [[a]] another current source that supplies a current to said differential pair,

wherein said differential pair includes a first and second input terminals, said first input terminal is a base of said first npn transistor, and said second input terminal is a base of said second npn transistor, and

wherein an emitter of said first npn transistor is connected to said another current source, and an emitter of said second npn transistor is connected to said another current source, the emitter of said first npn transistor being connected to the emitter of said second npn transistor.

11. (Currently Amended) The constant voltage generating circuit as claimed in claim 7 or 8,

wherein said differential amplifier has a differential pair including a first npn transistor and a second npn transistor having a larger emitter area than the first npn transistor, [[and]] a first and second current sources ~~that supplies~~ to supply a current to said differential pair, and said differential amplifier has a [[group]] second plurality of first npn transistors including m (an integer; 1≤m) first npn transistors, and a [[group]] second plurality of second npn transistors including m second npn transistors each having ~~a larger~~ an emitter area greater than the second plurality of m first npn transistor,

wherein said differential pair includes a first and second input terminals, said first input terminal is a base of said first npn transistor, and said second input terminal is a base of said second npn transistor, and

wherein an emitter of said first npn transistor is connected to said current source, and an emitter of said second npn transistor is connected to said current source, the emitter of said first npn transistor being connected to the emitter of said second npn transistor,

wherein a base and a collector of each of said [[group]] pluralities of first npn transistors are connected together, a collector of k (an integer; 2≤k≤m)-th one of the [[group]] second plurality of first npn transistor is connected to an emitter of a (k-1)-th one of the [[group]] second plurality of first npn transistors, the collector of a [[first]] one of said [[group]] second plurality of first npn transistors is connected to the emitter of the first npn transistor constituting said differential pair, and the emitter of an m-th one of

said [[group]] second plurality of first npn transistors is connected to said first current source, and

wherein a base and a collector of each of said [[group]] pluralities of second npn transistors are connected together, a collector of a k (an integer; $2 \leq k \leq m$)-th one of the [[group]] second plurality of second npn transistor is connected to an emitter of a (k-1)-th one of the [[group]] second plurality of second npn transistors, the collector of a [[first]] one of said [[group]] second plurality of second npn transistors is connected to the emitter of the second npn transistor constituting the differential pair, and the emitter of an m-th one of said [[group]] second plurality of second npn transistors is connected to said second current source.